REMARKS

Applicants respectfully request further examination and reconsideration in view of the above amendments. Claims 14-30 remain pending in the case. Claims 14-30 are rejected. Claim 14 has been cancelled without prejudice herein. Claims 15, 16, 19, 21 and 26-29 have been amended herein. No new matter has been added.

Attached hereto is a marked-up version of the changes made to the claims by the current amendments. The attachment is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

35 U.S.C. §112, second paragraph

Claims 16-18 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention. Applicants have amended Claim 16 herein to include the limitation of the gate comprising a polysilicon layer. This limitation is described in the present specification at page 5, lines 5-11. Specifically, polysilicon deposition gate is shown at step 212 of Figure 2 and at element 311 (polysilicon 1 layer 311). No new matter has been added.

Applicants respectfully assert that Claim 16, as amended, particularly points out and distinctly claims the subject matter Applicants regard as the invention, and

overcomes the rejection under 35 U.S.C. §112, second paragraph. Therefore, Applicants respectfully submit that Claims 17 and 18 which are dependent from Claim 16, also overcome the rejection under 35 U.S.C. §112, second paragraph.

35 U.S.C. §103(a)

Claims 15 and 19-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent 6,477,084 by Eitan, hereinafter the "Eitan" reference, in view of United States Patent 5,879,990 by Dormans, et al., hereinafter the "Dormans" reference. Applicant has reviewed the cited references and respectfully submit that the present invention as recited in Claims 15 and 19-30 is not anticipated nor rendered obvious by Eitan in view of Dormans.

Independent Claim 16 recites (emphasis added):

> A process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:
> forming a gate above said channel of said substrate, wherein said gate comprises a polysilicon layer;
> forming a bitline; and
> siliciding said bitline.

Claims 15 and 19-30 that depend from independent Claim 16 provide further recitations of the limitations of the present invention as claimed.

The combination of Eitan and Dormans does not teach a method for fabricating a memory cell comprising forming a gate above said channel of said substrate, wherein said gate comprises a polysilicon layer, prior to forming a bitline, as claimed. Eitan and these embodiments of the claimed invention are very different. Applicants understand Eitan to teach a NROM cell with a pocket implant self-aligned to at least one bit line junction. As pointed out by the Examiner, Eitan does not teach siliciding a bitline.

In particular, Eitan teaches forming a bitline prior to depositing the polysilicon on the gates. Applicants respectfully direct Examiner to Figure 7B of Eitan. Bit lines 104 are implanted between the columns of the bit line mask 168 through the oxide layer 160 (col. 8, lines 26-38). Subsequent to the bit line formation, polysilicon gates are deposited. In particular, Eitan states that "[t]he final step is the deposition of the polysilicon gates ..., in accordance with standard deposition techniques (col. 10, lines 16-18 and Figure 7F).

In contrast, embodiments of the claimed invention are directed towards forming a gate above said channel of said substrate, wherein said gate comprises a polysilicon layer, prior to forming a bitline, as claimed. In particular, a polysilicon layer is deposited as shown at step 212 of Figure 2 of the present invention (page 5, lines 5-11). Subsequently, the bitline is formed, as shown at step 220 of Figure 2 (page 6, lines 10-22).

Applicants respectfully assert that Eitan teaches a process of manufacturing a NROM cell wherein a bitline is formed prior to depositing the polysilicon on the gates. Therefore, Applicant respectfully asserts that Eitan not only does not suggest a process of fabricating a memory cell wherein polysilicon is deposited prior to bitline formation, as claimed, but rather teaches away from such a combination.

Moreover, the combination of Eitan and Dormans fails to teach or suggest this claim limitation because Dormans does not overcome the shortcomings of Eitan. Dormans, alone or in combination with Eitan, does not show or suggest a process of fabricating a memory cell comprising forming a gate above said channel of the substrate, wherein the gate comprises a polysilicon layer, prior to forming a bitline, as claimed. As described above, Eitan teaches manufacturing a NROM cell wherein a bitline is formed prior to depositing the polysilicon on the gates.

Applicants understand Dormans to teach a semiconductor device having an embedded non-volatile memory. Dormans does not teach, show or suggest fabricating a memory cell, as claimed. In particular, Dormans does not show or suggest a process of fabricating a memory cell comprising forming a gate above said channel of the substrate, wherein the gate comprises a polysilicon layer, prior to forming a bitline, as claimed.

In view of the claim limitation of forming a gate above said channel of the substrate, wherein the gate comprises a polysilicon layer, prior to forming a bitline not being shown or suggested in Dormans, in combination with the above arguments, Applicants respectfully submit that independent Claim 16 overcome the cited references and are therefore allowable over the combination of Eitan and Dormans.

Furthermore, Applicants respectfully assert that the combination of Eitan and Dormans is inoperative. In order to combine references, the references cannot be rendered unusable for their intended purpose. In particular, the NROM cell of Eitan comprises a thermally grown oxide layer over the bit lines. Eitan specifically recites that "[a] gate oxide layer is now thermally grown over the entire array using standard oxidation techniques" (col. 9, lines 52-54, emphasis added). "In the array, the oxidation step causes oxide, labeled 178 in Figure 7F, to grow over bit lines 104" (col. 9, lines 56-57).

In contrast, embodiments of the present invention are directed towards a process for fabricating a memory cell comprising siliciding a bitline, as claimed. In particular, as described in the present specification at page 7, lines 4-8, an oxide deposition is made on the bitline regions and the gate electrodes. The oxide deposition occurs subsequent to the silicidation of the bitline, as shown in Figure 2 at steps 226 and 228.

Applicants understand Dormans to form titanium silicide on the poly gates and the source and drain zones of the transistors under the influence of heating (col. 5, lines 24-26). Applicants respectfully assert that a silicide cannot be placed on a thermally grown oxide. As stated in Dormans (col. 5, lines 24-27), the titanium does not change into titanium silicide on the field oxide. Moreover, an oxide cannot be thermally grown over silicide, as the silicide would be destroyed. Rather, a mixed oxide of some nature would result.

Applicants respectfully assert that the silicide as described in Dormans cannot be placed on the bitline of Eitan, as the bitline of Eitan comprises a thermally grown oxide. Therefore, Applicants respectfully assert that the combination of Eitan and Dormans not only does not suggest a process of fabricating a memory cell comprising siliciding a bitline, as claimed, but rather such a combination is inoperable.

Claims 15 and 19-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Eitan and Dormans. Claims 15 and 19-30 are dependent on allowable base Claim 16. Applicants respectfully submit that Claims 15 and 19-30 overcome the Examiner's basis for rejection under 35 U.S.C. § 103(a) as these claims are dependent on an allowable base claim.

CONCLUSION

In light of the above remarks, Applicants respectfully request allowance of the present Application.

Applicants further respectfully point out that no contested Claims remain in the present Application.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge our deposit account No. 23-0085 for any unpaid fees.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claim 14 has been cancelled without prejudice.

Claim 15 has been amended as follows:

15. (Amended) The process of Claim [14] 16, comprising forming an oxide over said silicided bitline.

Claim 16 has been amended as follows:

16. (Amended) [The process of Claim 14, wherein prior to said forming a bitline] A process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:

forming a gate above said channel of said substrate, wherein said gate comprises a polysilicon layer [is formed over overlies said gate];

forming a bitline; and

siliciding said bitline.

Claim 19 has been amended as follows:

19. (Amended) The process of Claim [14] 16, comprising:

forming a charge trapping region that contains a first amount of charge; and

forming a layer between said channel and said charge trapping region, wherein said layer has a thickness such that said first amount of charge is prevented from directly tunneling into said layer.

Claim 21 has been amended as follows:

21. (Amended) The process of Claim [14] 16, wherein said gate comprises an N-type material.

Claim 26 has been amended as follows:

26. (Amended) The process of Claim [14] 16, wherein said memory cell comprises an EEPROM memory cell.

Claim 27 has been amended as follows:

27. (Amended) The process of Claim [14] 16, wherein said memory cell comprises a two-bit memory cell.

Claim 28 has been amended as follows:

28. (Amended) The process of Claim [14] 16, wherein said substrate comprises a P-type substrate.

Claim 29 has been amended as follows:

29. (Amended) The process of Claim [14] 16, further comprising scaling the length of said bitline.